

SANYO Semiconductors **DATA SHEET**

LC872H08A LC872H06A — LC872H04A

CMOS IC 8K/6K/4K-byte ROM and 256-byte RAM integrated 8-bit 1-chip Microcontroller

Overview

The SANYO LC872H08A/06A/04A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 8K/6K/4K-byte ROM, 256-byte RAM, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), two 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface, an asynchronous/synchronous SIO interface, a UART interface (full duplex), two 12-bit PWM channels, a 12/8-bit 9-channel AD converter, a system clock frequency divider, an internal reset and a 20-source 10-vector interrupt feature.

Features

■ROM

- 8192 × 8 bits (LC872H08A)
- 6144×8 bits (LC872H06A)
- 4096×8 bits (LC872H04A)

\blacksquare RAM

• 256 × 9 bits (LC872H08A/6A/4A)

■Minimum Bus Cycle

- 83.3ns (12MHz at V_{DD}=2.7V to 5.5V)
- 100ns (10MHz at V_{DD}=2.2V to 5.5V)
- 250ns (4MHz at V_{DD}=1.8V to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

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- ■Minimum Instruction Cycle Time
 - 250ns (12MHz at V_{DD}=2.7V to 5.5V)
 - 300ns (10MHz at V_{DD}=2.2V to 5.5V)
 - 750ns (4MHz at V_{DD}=1.8V to 5.5V)

■Ports

• Normal withstand voltage I/O ports

Ports I/O direction can be designated in 1-bit units
Ports I/O direction can be designated in 4-bit units

16 (Pin, P20, P21, P30, P31, P70 to P73)

8 (P0n)

• Dedicated oscillator ports/input ports 2 (CF1/XT1, CF2/XT2)

• Reset pin 1 (RES)

• Power pins 3 (VSS1, VSS2, VDD1)

■Timers

• Timer 0: 16-bit timer/counter with a capture register.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)

+ 8-bit counter (with an 8-bit capture register)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16-bit counter (with a 16-bit capture register)

• Timer 1: 16-bit timer/counter that supports PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)

(toggle outputs also possible from the lower-order 8 bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)

(The lower-order 8 bits can be used as PWM)

- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts are programmable in 5 different time schemes

■High-Speed Clock Counter

- Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- Can generate output real time.

■SIO

- SIO0: 8-bit Synchronous serial interface
 - 1) LSB first/MSB first mode selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3tCYC)
- SIO1: 8-bit asynchronous/synchronous serial interface
 - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART

- Full Duplex
- 7/8/9 bit data bits selectable
- 1 Stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator
- ■AD Converter: 12 bits/8 bits × 9 channels
 - 12/8 bits AD converter resolution selectable

■PWM: Multifrequency 12-bit PWM × 2 channels

- ■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
 - Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Clock Output Function

- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Can generate the source clock for the subclock

■Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts

- 20 sources, 10 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	ТОН
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- ■Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)
- High-speed Multiplication/Division Instructions

16 bits × 8 bits
24 bits × 16 bits
16 bits ÷ 8 bits
24 bits ÷ 16 bits
16 bits ÷ 8 bits
16 bits ÷ 16 bits
17 tCYC execution time
18 tCYC execution time
19 tCYC execution time
10 tCYC execution time
10 tCYC execution time
11 tCYC execution time
12 tCYC execution time
13 tCYC execution time
14 tCYC execution time
15 tCYC execution time
16 tCYC execution time
17 tCYC execution time
18 tCYC execution time
19 tCYC execution time
10 tCYC execution time

■Oscillation Circuits

• Internal oscillation circuits

Low-speed RC oscillation circuit : For system clock (100kHz)
Medium-speed RC oscillation circuit : For system clock (1MHz)
Multifrequency RC oscillation circuit : For system clock (8MHz)

• External oscillation circuits

Hi-speed CF oscillation circuit: For system clock, with internal Rf

Low speed crystal oscillation circuit: For low-speed system clock, with internal Rf

- 1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
- 2) Both the CF and crystal oscillator circuits stop operation on a system reset. When the reset is released, only the CF oscillation circuit resumes operation.

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■Internal Reset Function

- Power-on reset (POR) function
 - 1) POR reset is generated only at power-on time.
 - 2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
 - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
 - 2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) There are three ways of resetting the HALT mode.
 - (1) Setting the reset pin to the low level
 - (2) System resetting by watchdog timer or low-voltage detection
 - (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC and crystal oscillators automatically stop operation.
 - 2) There are four ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level.
 - (2) System resetting by watchdog timer or low-voltage detection
 - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
 - * INT0 and INT1 HOLD mode reset is available only when level detection is set.
 - (4) Having an interrupt source established at port 0.
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillator automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are five ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level.
 - (2) System resetting by watchdog timer or low-voltage detection.
 - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
 - * INT0 and INT1 HOLD mode reset is available only when level detection is set.
 - (4) Having an interrupt source established at port 0.
 - (5) Having an interrupt source established in the base timer circuit.

Note: Available only when X'tal oscillation is selected.

■Package Form

• QFP36 (7×7): Lead-free type

■Development Tools

• On-chip-debugger : TCB87 TypeB + LC87D2H08A

: TCB87 TypeB + LC87F2H08A

: TCB87 TypeC (3 wire version) + LC87D2H08A

: TCB87 TypeC (3 wire version) + LC87F2H08A

Note: LC87F2H08A has an On-chip debugger but its function is limited.

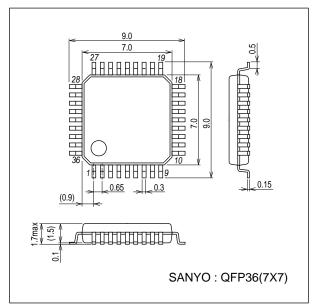
■Flash ROM Version

• LC87F2H08A

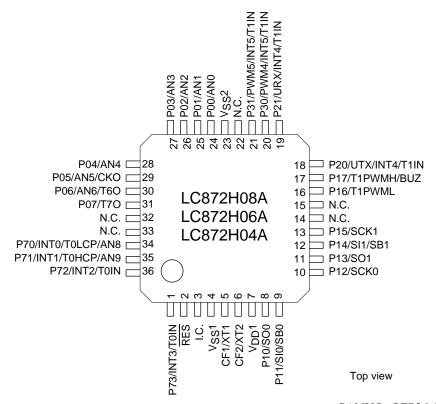
Package Dimensions

unit: mm (typ)

3162C



Pin Assignment



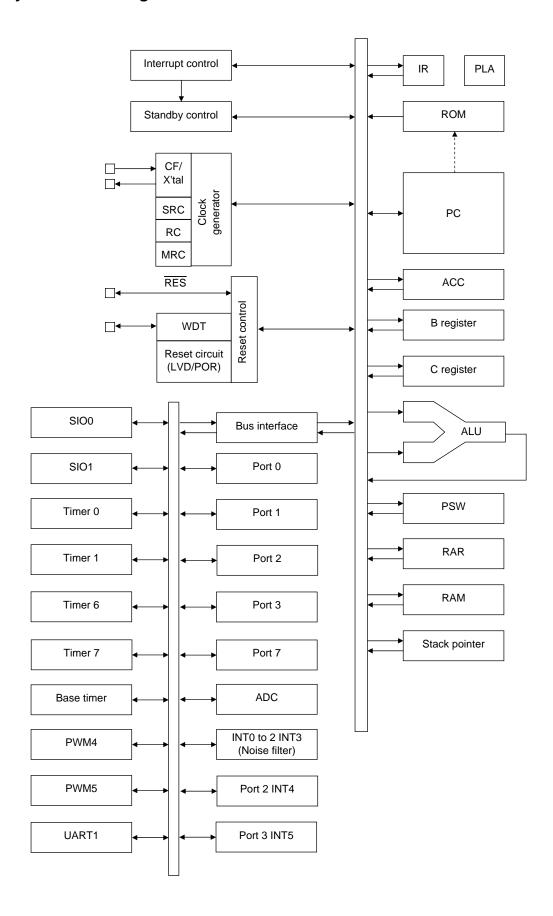
SANYO: QFP36 (7×7) "Lead-free Type"

QFP36	NAME
1	P73/INT3/T0IN
2	RES
3	I.C.
4	V _{SS} 1
5	CF1/XT1
6	CF2/XT2
7	V _{DD} 1
8	P10/SO0
9	P11/SI0/SB0
10	P12/SCK0
11	P13/SO1
12	P14/SI1/SB1
13	P15/SCK1
14	N.C.
15	N.C.
16	P16/T1PWML
17	P17/T1PWMH/BUZ
18	P20/UTX/INT4/T1IN

QFP36	NAME
19	P21/URX/INT4/T1IN
20	P30/PWM4/INT5/T1IN
21	P31/PWM5/INT5/T1IN
22	N.C.
23	V _{SS} 2
24	P00/AN0
25	P01/AN1
26	P02/AN2
27	P03/AN3
28	P04/AN4
29	P05/AN5/CKO
30	P06/AN6/T6O
31	P07/T7O
32	N.C.
33	N.C.
34	P70/INT0/T0LCP/AN8
35	P71/INT1/T0HCP/AN9
36	P72/INT2/T0IN

Note I.C. and N.C. pins must be held open (disconnected).

System Block Diagram



Pin Description

Pin Name	I/O			Des	scription			Option	
V _{SS} 1,V _{SS} 2	-	- power supply pir	ns					No	
V _{DD} 1	-	+ power supply pi	+ power supply pin						
Port 0	I/O	• 8-bit I/O port							
P00 to P07		I/O specifiable in	n 4-bit units						
		Pull-up resistors	can be turned	on and off in 4	-bit units.				
		HOLD reset inp							
		Port 0 interrupt	input					Vaa	
		Pin functions						Yes	
		P05: System clo	ck output						
		P06: Timer 6 tog	ggle output						
		P07: Timer 7 tog	ggle output						
		P00(AN0) to P0	6(AN6):AD con	verter input					
Port 1	I/O	• 8-bit I/O port							
P10 to P17		I/O specifiable in	n 1-bit units						
		Pull-up resistors	can be turned	on and off in 1	-bit units.				
		 Pin functions 						Yes	
		P10: SIO0 data	output	P14	l: SIO1 data inpu	t/bus I/O		103	
		P11: SIO0 data	input/bus I/O	P15	: SIO1 clock I/O				
		P12: SIO0 clock	I/O		6: Timer 1 PWML	•			
		P13: SIO1 data	output	P17	: Timer 1 PWMF	l output/beeper	output		
Port 2	I/O	• 2-bit I/O port							
P20 to P21		I/O specifiable in							
		Pull-up resistors	can be turned	on and off in 1	-bit units.				
		Pin functions							
		P20: UART tran							
		P21: UART rece							
			-		r 1 event input/tir	ner 0L capture	nput/	Yes	
			er 0H capture in	nput					
		Interrupt acknow	vieage types						
			Rising	Falling	Rising &	H level	L level		
					Falling				
		INT4	enable	enable	enable	disable	disable		
Port 3	I/O	• 2-bit I/O port							
P30 to P31		I/O specifiable in	n 1-bit units						
		Pull-up resistors	can be turned	on and off in 1	-bit units.				
		 Pin functions 							
		P30: PWM4 out	put						
		P31: PWM5 out							
			•	•	r 1 event input/tir	ner 0L capture i	nput/	Yes	
			er 0H capture i	nput					
		Interrupt acknow	vledge types		1	T	1		
			Rising	Falling	Rising &	H level	L level		
		INT5	enable	onabla	Falling	disable	disable		
		INIS	enable	enable	enable	disable	disable		

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Pin Name	I/O			Des	cription			Option	n
Port 7	I/O	• 4-bit I/O port	·						
P70 to P73		· ·	O specifiable in 1-bit units						
		 Pull-up resistor 	s can be turned	on and off in 1-	bit units.				
		 Pin functions 							
		P70: INT0 input	HOLD reset in	put/timer 0L cap	ture input/watch	dog timer outpu	t		
		P71: INT1 input	HOLD reset in	put/timer 0H cap	ture input				
		P72: INT2 input	HOLD reset in	put/timer 0 even	t input/timer 0L o	capture input			
		P73: INT3 inpu	t (input with nois	se filter)/timer 0	event input/time	OH capture inp	ut		
		P70(AN8),P71(AN9) : AD conv	erter input				No	
		Interrupt acknow	wledge types					140	
			Rising	Falling	Rising &	H level	L level		
			rtioning	1 dilling	Falling	1110401	2 10101		
		INT0	enable	enable	disable	enable	enable		
		INT1	enable	enable	disable	enable	enable		
		INT2	enable	enable	enable	disable	disable		
		INT3	enable	enable	enable	disable	disable		
RES	I/O	External reset In	out/internal rese	et output				No	
CF1/XT1	T .	Ceramic resonate	ator or 32.768kH	Iz crystal oscilla	tor input pin				
0	1	Pin function	210. 0. 0200	0.70.0. 0000	toput p			No	
		General-purpose	input port						
CF2/XT2	I/O	Ceramic resona		Iz crystal oscilla	tor output pin				
		Pin function		,				No	
		General-purpose	input port						

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P31	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

User Option Table

Option Name	Option to be Applied on	Mask-ROM Version *1	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	0	0	1 bit	CMOS
					Nch-open drain
	P10 to P17	0	0	1 bit	CMOS
					Nch-open drain
	P20 to P21	0	0	1 bit	CMOS
					Nch-open drain
	P30 to P31	0	0	1 bit	CMOS
					Nch-open drain
Program start	-	×	0	-	00000h
address		*2			01E00h
Low-voltage	Detect function	0	0	-	Enable:Use
detection reset					Disable:Not Used
function	Detect level	0	0	-	7-level
Power-on reset function	Power-On reset level	0	0	-	8-level

^{*1:} Mask option selection – No change possible after mask is completed.

Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections					
Port Name	Board	Software				
P00 to P07	Open	Output low				
P10 to P17	Open	Output low				
P20 to P21	Open	Output low				
P30 to P31	Open	Output low				
P70 to P73	Open	Output low				
CF1/XT1	Pulled low with a 100kΩ resistor or less	General-purpose input port				
CF2/XT2	Pulled low with a 100kΩ resistor or less	General-purpose input port				

Notes on CF1/XT1 and CF2/XT2 pins

• When using as general-purpose input ports Since the CF1/XT1 and CF2/XT2 pins are configured as CF oscillator pins at system reset time, it is necessary to add a current limiting resistor of $1k\Omega$ or greater to the CF2/XT2 pin in series when using them as general-purpose input pins.

• Differences between flash and mask ROM version

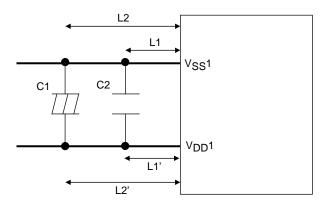
		System Reset Time State	After System Reset is Released
Flash ROM version	CF1/XT1	Set high via the internal Rf resistor	CF oscillation state
LC87F2H08A	CF2/XT2	Set high	CF oscillation state
Mask ROM version	CF1/XT1	Set low via the internal Rf resistor	CF oscillation state
LC872H08A/06A/04A	CF2/XT2	Set low	CF oscillation state

^{*2:} Program start address of the mask version is 00000h.

Power Pin Treatment Recommendations (VDD1, VSS1)

Connect bypass capacitors that meet the following conditions between the VDD1 and VSS1 pins:

- Connect among the V_{DD}1 and V_{SS}1 pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as equal as possible (L1=L1', L2=L2').
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1μF.



Note: Be sure to electrically short-circuit between the VSS1 and VSS2 pins.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$

			T	7 55 55					
	Parameter	Symbol	Pin/Remarks	Conditions		. 1	Specifi		
		.,			V _{DD} [V]	min	typ	max	unit
	ximum supply tage	V _{DD} max	V _{DD} 1			-0.3		+6.5	
Inp	ut voltage	VI	CF1, CF2			-0.3		V _{DD} +0.3	V
	ut/output tage	V _{IO}	Ports 0, 1, 2, 3 Port 7			-0.3		V _{DD} +0.3	
	Peak output current	IOPH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-10			
Ħ		IOPH(2)	P71 to P73	Per 1 applicable pin		-5			
High level output current	Mean output current	IOMH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-7.5			
utbn	(Note 1-1)	IOMH(2)	P71 to P73	Per 1 applicable pin		-3			
vel c	Total output	ΣΙΟΑΗ(1)	P71 to P73	Total of all applicable pins		-10			
jh le	current	ΣΙΟΑΗ(2)	P10 to P14	Total of all applicable pins		-20			
H		ΣΙΟΑΗ(3)	P15 to P17 Ports 0, 2, 3	Total of all applicable pins		-20			
		ΣΙΟΑΗ(4)	Ports 0, 1, 2, 3	Total of all applicable pins		-25			
	Peak output	IOPL(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin				20	mA
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Port 7	Per 1 applicable pin				10	
Low level output current	Mean output	IOML(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin				15	
rtput	(Note 1-1)	IOML(2)	P00, P01	Per 1 applicable pin				20	
no le		IOML(3)	Port 7	Per 1 applicable pin				7.5	
v lev	Total output	ΣIOAL(1)	Port 7	Total of all applicable pins				15	
Lo	current	ΣIOAL(2)	Port 0	Total of all applicable pins				40	
		ΣIOAL(3)	P10 to P14	Total of all applicable pins				35	
		ΣIOAL(4)	Ports 1, 2, 3	Total of all applicable pins				40	
		ΣIOAL(5)	Ports 0, 1, 2, 3	Total of all applicable pins				70	
	wer ssipation	Pd max(1)	QFP36(7×7)	Ta=-40 to +85°C Package only				120	
	ораноп	Pd max(2)		Ta=-40 to +85°C Package with thermal resistance board (Note 1-2)				265	mW
	erating ambient	Topr				-40		+85	
Sto	orage ambient	Tstg				-55		+125	°C

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Allowable Operating Conditions at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	I Pin/Remarks Conditions			Specification			
Farameter	Symbol	FIII/Nemarks	Conditions	V _{DD} [V]	min	typ	max	unit
Operating	V _{DD} (1)	V _{DD} 1	0.245μs ≤ tCYC ≤ 200μs		2.7		5.5	
supply voltage	V _{DD} (2)		$0.294\mu s \le tCYC \le 200\mu s$		2.2		5.5	
	V _{DD} (3)		$0.735\mu s \le tCYC \le 200\mu s$		1.8		5.5	
Memory sustaining supply voltage	VHD	V _{DD} 1	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	V _{IH} (1)	Ports 1, 2, 3, P71 to P73 P70 port input/ interrupt side		1.8 to 5.5	0.3V _{DD} +0.7		V _{DD}	
	V _{IH} (2)	Ports 0		1.8 to 5.5	0.3V _{DD} +0.7		V_{DD}	
	V _{IH} (3)	Port 70 watchdog timer side		1.8 to 5.5	0.9V _{DD}		V _{DD}	٧
	V _{IH} (4)	CF1, RES		1.8 to 5.5	0.75V _{DD}		V_{DD}	
Low level	V _{IL} (1)	Ports 1, 2, 3,		4.0 to 5.5	V _{SS}		0.1V _{DD} +0.4	
input voltage		P71 to P73 P70 port input/ interrupt side		1.8 to 4.0	V _{SS}		0.2V _{DD}	
	V _{IL} (2)	Ports 0		4.0 to 5.5	V _{SS}		0.15V _{DD} +0.4	}
				1.8 to 4.0	VSS		0.2V _{DD}	
	V _{IL} (3)	Port 70 watchdog timer side		1.8 to 5.5	V _{SS}		0.8V _{DD} -1.0	
	V _{IL} (4)	CF1, RES		1.8 to 5.5	V _{SS}		0.25V _{DD}	
Instruction	tCYC	,,,,,,		2.7 to 5.5	0.245		200	
cycle time	(Note 2-1)			2.2 to 5.5	0.294		200	μs
				1.8 to 5.5	0.735		200	μο
External	FEXCF	CF1	CF2 pin open	2.7 to 5.5	0.733		12	
system clock frequency	. 2/13/		System clock frequency division ratio=1/1	1.8 to 5.5	0.1		4	
			External system clock duty=50±5% CF2 pin open	204-55	0.0		04.4	MHz
			System clock frequency division ratio=1/2 External system clock duty=50±5%	3.0 to 5.5 2.0 to 5.5	0.2		24.4	
Oscillation frequency	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		12		
range (Note 2-2)	FmCF(2)	CF1, CF2	10MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		10		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation. CF oscillation normal amplifier size selected. (CFLAMP=0) See Fig. 1.	1.8 to 5.5		4		
			4MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1.	2.2 to 5.5		4		MHz
	FmMRC		Frequency variable RC oscillation. 1/2 frequency division ratio. (RCCTD=0) (Note 2-3)	2.7 to 5.5	7.44	8.0	8.56	
	FmRC		Internal medium-speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	1.8 to 5.5	50	100	200	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	1.8 to 5.5		32.768		kHz
	1	1	<u>. </u>					

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: When switching the system clock, allow an oscillation stabilization time of 100µs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

Note 2-2: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = V_{SS}2 = 0V$

			, 55	55				
Doromotor	Cumhal	Din/Damarks	Conditions			Specifica	ition	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1, 2, 3 Port 7 RES	Output disabled Pull-up resistor off VIN=VDD (Including output Tr's off leakage current)	1.8 to 5.5			1	
	I _{IH} (2)	CF1	$V_{IN}=V_{DD}$	1.8 to 5.5			15	
Low level input current	I _{IL} (1)	Ports 0, 1, 2, 3 Port 7 RES	Output disabled Pull-up resistor off VIN=VSS (Including output Tr's off leakage current)	1.8 to 5.5	-1			μΑ
	I _{IL} (2)	CF1	V _{IN} =V _{SS}	1.8 to 5.5	-15			
High level output	V _{OH} (1)	Ports 0, 1, 2	I _{OH} =-1mA	4.5 to 5.5	V _{DD} -1			
voltage	V _{OH} (2)	P71 to P73	I _{OH} =-0.35mA	2.7 to 5.5	V _{DD} -0.4			
	V _{OH} (3)		I _{OH} =-0.15mA	1.8 to 5.5	V _{DD} -0.4			
	V _{OH} (4)	Port 3	I _{OH} =-6mA	4.5 to 5.5	V _{DD} -1			
	V _{OH} (5)		I _{OH} =-1.4mA	2.7 to 5.5	V _{DD} -0.4			
	V _{OH} (6)		I _{OH} =-0.8mA	1.8 to 5.5	V _{DD} -0.4			
Low level output	V _{OL} (1)	Ports 0, 1, 2, 3	I _{OL} =10mA	4.5 to 5.5			1.5	V
voltage	V _{OL} (2)		I _{OL} =1.4mA	2.7 to 5.5			0.4	V
	V _{OL} (3)		I _{OL} =0.8mA	1.8 to 5.5			0.4	
	V _{OL} (4)	Port 7	I _{OL} =1.4mA	2.7 to 5.5			0.4	
	V _{OL} (5)		I _{OL} =0.8mA	1.8 to 5.5			0.4	
	V _{OL} (6)	P00, P01	I _{OL} =25mA	4.5 to 5.5			1.5	
	V _{OL} (7)		I _{OL} =4mA	2.7 to 5.5			0.4	
	V _{OL} (8)		I _{OL} =2mA	1.8 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	V _{OH} =0.9V _{DD} When Port 0 selected	4.5 to 5.5	15	35	80	
	Rpu(2)	1 Oit 7	low-impedance pull-up.	1.8 to 4.5	18	50	230	
	Rpu(3)	Port 0	V _{OH} =0.9V _{DD} When Port 0 selected high-impedance pull-up.	1.8 to 5.5	100	210	400	kΩ
Hysteresis voltage	VHYS(1)	Ports 1, 2, 3, 7		2.7 to 5.5		0.1V _{DD}		V
	VHYS(2)	RES		1.8 to 2.7		0.07V _{DD}		v
Pin capacitance	СР	All pins	For pins other than that under test: VIN=VSS f=1MHz Ta=25°C	1.8 to 5.5		10		pF

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

	-	Parameter	Cumbal	Pin/	Conditions			Speci	fication	
	r	Parameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
		Frequency	tSCK(1)	SCK0(P12)	• See Fig. 5.		2			
	Input clock	Low level	tSCKL(1)				1			
	ont o	pulse width				1.8 to 5.5				tCYC
ock	ī	High level	tSCKH(1)				1			
Serial clock		pulse width	1001(10)	001(0(010)	01100					
Seri	쓩	Frequency	tSCK(2)	SCK0(P12)	CMOS output selected		4/3			
"	Low level tSCKL(2) pulse width High level tSCKH(2)		tSCKL(2)		• See Fig. 5.	1.8 to 5.5		1/2		
	ntpn		+CCK1 (/0)	+		1.6 10 5.5				tSCK
	Õ	High level pulse width	tSCKH(2)					1/2		
Serial input	Da	ta setup time	tsDI(1)	SB0(P11), SI0(P11)	Must be specified with respect to rising edge of SIOCLK.	1.8 to 5.5	0.05			
Seria	Da	ta hold time	thDI(1)	-	• See Fig. 5.	1.8 to 3.5	0.05			
	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	Continuous data transmission/reception mode (Note 4-1-2)				(1/3)tCYC +0.08	μs
Serial output	Inp		tdD0(2)		• Synchronous 8-bit mode (Note 4-1-2)	1.8 to 5.5			1tCYC +0.08	
Serial	Output clock		tdD0(3)		(Note 4-1-2)	1.0 to 3.5			(1/3)tCYC +0.08	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

		Doromotor	Cumbal	Pin/	Conditions			Spec	fication	
		Parameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
	¥	Frequency	tSCK(3)	SCK1(P15)	See Fig. 5.		2			
	Input clock	Low level pulse width	tSCKL(3)			1.8 to 5.5	1			
clock	ū	High level pulse width	tSCKH(3)				1			tCYC
Serial clock	충	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected See Fig. 5.		2			
	Output clock	Low level pulse width	tSCKL(4)			1.8 to 5.5		1/2		tSCK
	ŏ	High level pulse width	tSCKH(4)					1/2		ISCK
Serial input	Da	ata setup time	tsDI(2)	SB1(P14), SI1(P14)	Must be specified with respect to rising edge of SIOCLK. See Fig. 5.	400.55	0.05			
Serial	Da	ata hold time	thDI(2)			1.8 to 5.5	0.05			
Serial output		utput delay time	tdD0(4)	SO1(P13), SB1(P14)	Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.	1.8 to 5.5			(1/3)tCYC +0.08	μs

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			Speci	fication	
Farameter	Syllibol	Fill/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High/low level	tPIH(1)	INT0(P70),	Interrupt source flag can be set.					
pulse width	tPIL(1)	INT1(P71),	Event inputs for timer 0 or 1 are					
		INT2(P72),	enabled.	1.8 to 5.5	1			
		INT4(P20 to P21),						
		INT5(P30 to P31)						
	tPIH(2)	INT3(P73) when noise	Interrupt source flag can be set.					
	tPIL(2)	filter time constant is	Event inputs for timer 0 are	1.8 to 5.5	2			40)/0
		1/1	enabled.					tCYC
	tPIH(3)	INT3(P73) when noise	Interrupt source flag can be set.					
	tPIL(3)	filter time constant is	Event inputs for timer 0 are	1.8 to 5.5	64			
		1/32	enabled.					
	tPIH(4)	INT3(P73) when noise	Interrupt source flag can be set.					
	tPIL(4)	filter time constant is	Event inputs for timer 0 are	1.8 to 5.5	256			
		1/128	enabled.					
	tPIL(5)	RES	Resetting is enabled.	1.8 to 5.5	200			μs

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = 0V$

<12bits AD Converter Mode/Ta = -40°C to +85°C >

Danasatas	Oh!	Dia /Damania	O and distance			Specific	cation	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to		2.4 to 5.5		12		bit
Absolute	ET	AN6(P06),	(Note 6-1)	3.0 to 5.5			±16	LCD
accuracy		AN8(P70),	(Note 6-1)	2.4 to 3.6			±20	LSB
Conversion time	TCAD	AN9(P71)	See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	
				3.0 to 5.5	64		115	μs
		See Conversion time calculation formulas. (Note 6-2)	2.4 to 3.6	410		425	μο	
Analog input voltage range	VAIN			2.4 to 5.5	V _{SS}		V_{DD}	>
Analog port	IAINH		VAIN=V _{DD}	2.4 to 5.5		·	1	
	IAINL		VAIN=V _{SS}	2.4 to 5.5	-1		·	μΑ

<8bits AD Converter Mode/Ta = -40°C to +85°C >

	0	D: /D	0 - 10			Specifi	cation	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to		2.4 to 5.5		8		bit
Absolute accuracy	ET	AN6(P06) AN8(P70)	(Note 6-1)	2.4 to 5.5			±1.5	LSB
Conversion time	onversion time TCAD AN9(P71)	AN9(P71)	formulae (Note 6.2)	4.0 to 5.5	20		90	
				3.0 to 5.5	40		90	μs
			See Conversion time calculation formulas. (Note 6-2)	2.4 to 3.6	250		265	μσ
Analog input voltage range	VAIN			2.4 to 5.5	V _{SS}		V _{DD}	V
	IAINH		VAIN=V _{DD}	2.4 to 5.5			1	0
input current	t current IAINL	VAIN=V _{SS}	2.4 to 5.5	-1			μΑ	

Conversion time calculation formulas:

12bits AD Converter Mode: TCAD(Conversion time) = $((52/(AD \text{ division ratio}))+2)\times(1/3)\times tCYC$ 8bits AD Converter Mode: TCAD(Conversion time) = $((32/(AD \text{ division ratio}))+2)\times(1/3)\times tCYC$

External oscillation	Operating supply voltage range	System division ratio	Cycle time	AD division ratio	AD conversion time (TCAD)		
(FmCF)	(V _{DD})	(SYSDIV)	(tCYC)	(ADDIV)	12bit AD	8bit AD	
CF-12MHz	4.0V to 5.5V	1/1	250ns	1/8	34.8µs	21.5μs	
CF-12IVIHZ	3.0V to 5.5V	1/1	250ns	1/16	69.5µs	42.8µs	
CF-10MHz	4.0V to 5.5V	1/1	300ns	1/8	41.8µs	25.8µs	
CF-10IVIEZ	3.0V to 5.5V	1/1	300ns	1/16	83.4µs	51.4µs	
OF AMILE	3.0V to 5.5V	1/1	750ns	1/8	104.5μs	64.5µs	
CF-4MHz	2.4V to 3.6V	1/1	750ns	1/32	416.5μs	256.5μs	

Note 6-1: The quantization error $(\pm 1/2LSB)$ must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, $V_{SS}1=V_{SS}2=0V$

						Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit
POR release	PORRL		Select from option.	1.67V	1.55	1.67	1.79	
voltage			(Note 7-1)	1.97V	1.85	1.97	2.09	
				2.07V	1.95	2.07	2.19	
				2.37V	2.25	2.37	2.49	
				2.57V	2.45	2.57	2.69	
				2.87V	2.75	2.87	2.99	V
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS		• See Fig. 7. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		Power supply rise time from 0V to 1.6V.				100	ms

Note7-1: The POR release level can be selected out of 8 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

Low Voltage Detection Reset (LVD) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V

		,			10 0 10 1	Specific		_
Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit
LVD reset Voltage	LVDET		Select from option.	1.91V	1.81	1.91	2.01	
(Note 8-2)			(Note 8-1)	2.01V	1.91	2.01	2.11	
			(Note 8-3) • See Fig. 8.	2.31V	2.21	2.31	2.41	
			• See Fig. 6.	2.51V	2.41	2.51	2.61	V
				2.81V	2.71	2.81	2.91	
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD hysteresys	LVHYS			1.91V		55		
width				2.01V		55		
				2.31V		55		
				2.51V		55		mV
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		• See Fig. 8. (Note 8-4)			0.7	0.95	٧
Low voltage detection minimum Width (Reply sensitivity)	TLVDW		• LVDET-0.5V • See Fig. 9.		0.2			ms

Note8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

Consumption Current Characteristics at Ta = -40 °C to +85 °C, $V_{SS}1 = V_{SS}2 = 0V$

		Pin/		, , , <u>, , , , , , , , , , , , , , , , </u>		Specif	ication	
Parameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Normal mode consumption current	IDDOP(1)	V _{DD} 1	FmCF=12MHz ceramic oscillation mode System clock set to 12MHz side Internal low speed and medium speed RC	2.7 to 5.5		6.2	10.5	
(Note 9-1) (Note 9-2)			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		3.5	5.8	
	IDDOP(2)		CF1=24MHz external clock System clock set to CF1 side Internal low speed and medium speed RC	3.0 to 5.5		6.6	11.2	
			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 3.6		3.8	6.3	
	IDDOP(3)		FmCF=10MHz ceramic oscillation mode System clock set to 10MHz side Internal low speed and medium speed RC	2.2 to 5.5		5.3	9.5	
			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 3.6		3.0	5.3	
	IDDOP(4)		FmCF=4MHz ceramic oscillation mode System clock set to 4MHz side Internal low speed and medium speed RC	1.8 to 5.5		2.5	5.5	
			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 3.6		1.3	2.7	mA
	IDDOP(5)		CF oscillation low amplifier size selected. (CFLAMP=1) FmCF=4MHz ceramic oscillation mode System clock set to 4MHz side	2.2 to 5.5		0.9	2.2	
			Internal low speed and medium speed RC oscillation stopped. Frequency variable RC oscillation stopped. 1/4 frequency division ratio	2.2 to 3.6		0.5	1.0	
	IDDOP(6)		FsX'tal=32.768kHz crystal oscillation mode Internal low speed RC oscillation stopped. System clock set to internal medium speed	1.8 to 5.5		0.5	1.3	
			RC oscillation. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 3.6		0.3	0.6	
	IDDOP(7)		FsX'tal=32.768kHz crystal oscillation mode Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		4.2	8.8	
			System clock set to 8MHz with frequency variable RC oscillation 1/1 frequency division ratio	2.7 to 3.6		2.6	5.0	
	IDDOP(8)		External FsX'tal and FmCF oscillation stopped. System clock set to internal low speed RC oscillation.	1.8 to 5.5		55	197	
			Internal medium speed RC oscillation sopped. Frequency variable RC oscillation stopped. 1/1 frequency division ratio	1.8 to 3.6		33	108	
	IDDOP(9)		External FsX'tal and FmCF oscillation stopped. System clock set to internal low speed RC oscillation.	5.0		55	153	μА
			Internal medium speed RC oscillation sopped. Frequency variable RC oscillation stopped.	3.3		33	90	
			1/1 frequency division ratio Ta=-10 to +50°C	2.5		23	64	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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Continued from		Pin/	Conditions			Specif	fication	
Parameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Normal mode consumption current	IDDOP(10)	V _{DD} 1	FsX'tal=32.768kHz crystal oscillation mode System clock set to 32.768kHz side Internal low speed and medium speed RC	1.8 to 5.5		33	101	
(Note 9-1) (Note 9-2)			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 3.6		12	41	
	IDDOP(11)		FsX'tal=32.768kHz crystal oscillation mode System clock set to 32.768kHz side	5.0		33	68	μΑ
			Internal low speed and medium speed RC oscillation stopped.	3.3		12	27	
			Frequency variable RC oscillation stopped. 1/2 frequency division ratio Ta=-10 to +50°C	2.5		6.1	15	
HALT mode consumption current	IDDHALT(1)	V _{DD} 1	HALT mode FmCF=12MHz ceramic oscillation mode System clock set to 12MHz side	2.7 to 5.5		2.5	4.4	
(Note 9-1) (Note 9-2)			Internal low speed and medium speed RC oscillation stopped. Frequency variable RC oscillation stopped. 1/1 frequency division ratio	2.7 to 3.6		1.3	2.1	
	IDDHALT(2)		HALT mode CF1=24MHz external clock System clock set to CF1 side Internal low speed and medium speed RC	3.0 to 5.5		2.8	4.8	
			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 3.6		1.6	2.6	
	IDDHALT(3)		HALT mode FmCF=10MHz ceramic oscillation mode System clock set to 10MHz side Internal low speed and medium speed RC	2.2 to 5.5		2.2	3.9	
			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 3.6		1.1	1.9	
	IDDHALT(4)		HALT mode FmCF=4MHz ceramic oscillation mode System clock set to 4MHz side Internal low speed and medium speed RC	1.8 to 5.5		1.3	3.1	mA
			oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 3.6		0.6	1.2	
	IDDHALT(5)		HALT mode CF oscillation low amplifier size selected. (CFLAMP=1) FmCF=4MHz ceramic oscillation mode System clock set to 4MHz side	2.2 to 5.5		0.6	1.6	
			Internal low speed and medium speed RC oscillation stopped. Frequency variable RC oscillation stopped. 1/4 frequency division ratio	2.2 to 3.6		0.3	0.6	
	IDDHALT(6)		HALT mode FsX'tal=32.768kHz crystal oscillation mode Internal low speed RC oscillation stopped. System clock set to internal medium speed	1.8 to 5.5		0.3	0.9	
			System clock set to internal medium speed RC oscillation Frequency variable RC oscillation stopped. 1/2 frequency division ratio	1.8 to 3.6		0.2	0.4	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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MALT mode Consumption Check Consumption Check Chec	Parameter	Symbol	Pin/	Conditions			Specif	ication	
Fix/timel-32/788Hz/z crystal oscillation mode Fix/timel-32/788Hz/z crystal oscillation mode System clock set to 8MHz with Independent System clock set to 8MHz with System clock set to 3MHz with System clock System clock set to 3MHz with System clock System clock set to 3MHz with System clock S	T didiliotoi	Cymbol	remarks	CONGRESIO	V _{DD} [V]	min	typ	max	unit
IDDHALT(8) IDD	consumption current	IDDHALT(7)	V _{DD} 1	FsX'tal=32.768kHz crystal oscillation mode Internal low speed and medium speed RC	2.7 to 5.5		1.6	3.5	mA
IDDHALT(8)	,			System clock set to 8MHz with frequency variable RC oscillation	2.7 to 3.6		1.1	2.0	
IDDHALT(19) IDDHALT(19) IDDHALT(10) IDDHALT(10) IDDHALT(10) IDDHALT(10) IDDHALT(10) IDDHALT(10) IDDHALT(10) IDDHALT(10) IDDHALT(10) IDDHALT(11)		IDDHALT(8)		HALT mode External FsX'tal and FmCF oscillation stopped. System clock set to internal low speed RC	1.8 to 5.5		19	88	
External FaXtal and FmCF oscillation stopped. 5.0 19 55				Internal medium speed RC oscillation sopped. Frequency variable RC oscillation stopped. 1/1 frequency division ratio			11	46	
IDDHALT(10) IDDHALT(11)		IDDHALT(9)		External FsX'tal and FmCF oscillation stopped.	5.0		19	55	
IDDHALT(10)				oscillation. • Internal medium speed RC oscillation sopped.	3.3		11	32	
IDDHALT(10)				1/1 frequency division ratio	2.5		7.7	22	
DDHALT(11) Frequency variable RC oscillation stopped. 1.8 to 3.6 8.5 38			FsX'tal=32.768kHz crystal oscillation mo System clock set to 32.768kHz side Internal low speed and medium speed R	FsX'tal=32.768kHz crystal oscillation mode System clock set to 32.768kHz side	1.8 to 5.5		27	100	μА
FSX'tal=32.768kHz crystal oscillation mode				oscillation stopped. • Frequency variable RC oscillation stopped.	1.8 to 3.6		8.5	38	
IDDHOLD(1) IDDHOLD(2) IDDHOLD(3) IDDHOLD(4) IDDHOLD(4) IDDHOLD(4) IDDHOLD(4) IDDHOLD(5) IDDHOLD(5) IDDHOLD(5) IDDHOLD(5) IDDHOLD(5) IDDHOLD(5) IDDHOLD(5) IDDHOLD(6) ID			FsX'tal=32.768kHz crystal oscillation mode	5.0		27	65		
HOLD mode consumption current (Note 9-1)				Internal low speed and medium speed RC oscillation stopped.	3.3		8.5	23	
CF1=V _{DD} or open (External clock mode) 1.8 to 3.6 0.01 9.0				• 1/2 frequency division ratio	2.5		3.8	11	
Current (Note 9-1) (Note 9-2) IDDHOLD(2) HOLD mode 5.0 0.02 1.7 (Note 9-2) IDDHOLD(3) Ta=-10 to +50°C 2.5 0.009 0.6 IDDHOLD(3) HOLD mode 1.8 to 5.5 3.0 23 LVD option selected 1.8 to 3.6 2.3 12 HOLD mode 5.0 3.0 5.7 LVD option selected 5.0 3.0 5.7 CF1=Vpp or open (External clock mode) 3.3 2.3 3.9 Ta=-10 to +50°C 2.5 2.0 3.3 Timer HOLD mode 1.8 to 5.5 22 95 LVD option selected 1.8 to 5.5 22 95 Timer HOLD mode 1.8 to 3.6 7.5 35 Timer HOLD mode 5.0 22 60 FSX'tal=32.768kHz crystal oscillation mode 5.0 22 60 FSX'tal=32.768kHz crystal oscillation mode 3.3 7.5 21 Tall to to +50°C 7.5 21		IDDHOLD(1)	V _{DD} 1		1.8 to 5.5		0.02	20	
Note 9-1) (Note 9-2) Note 9-2) Not	•			CF1=V _{DD} or open (External clock mode)	1.8 to 3.6		0.01	9.0	
(Note 9-2) IDDHOLD(3) Ta=-10 to +50°C 2.5 0.009 0.6 HOLD mode 1.8 to 5.5 3.0 23 LVD option selected HOLD mode 1.8 to 3.6 2.3 12 HOLD mode 5.0 3.0 5.7 CF1=V _{DD} or open (External clock mode) 1.8 to 3.6 2.3 3.9 Ta=-10 to +50°C 2.5 2.0 3.3 Timer HOLD mode 5.0 3.0 5.7 LVD option selected 2.5 2.0 3.3 Timer HOLD mode 1.8 to 5.5 22 95 FSX'tal=32.768 kHz crystal oscillation mode 5.0 22 60 Timer HOLD mode 5.0 22 60 FSX'tal=32.768kHz crystal oscillation mode 3.3 7.5 21 Timer HOLD mode 5.0 22 60 FSX'tal=32.768kHz crystal oscillation mode 5.0 22 60 Ta=-10 to +50°C 7.5 21 Ta=-10 to +50°C 7.5 7.5 21 Ta=-10 to +50°C 7.5 7.5 7.5 Ta=-10 to +50°C 7.5 7.5 7.5		IDDHOLD(2)			5.0		0.02	1.7	
IDDHOLD(3)				_ ==	3.3		0.01	8.0	
CF1=V _{DD} or open (External clock mode)					2.5		0.009	0.6	
LVD option selected 1.8 to 3.6 2.3 12		IDDHOLD(3)			1.8 to 5.5		3.0	23	
CF1=VDD or open (External clock mode) 3.3 2.3 3.9 Ta=-10 to +50°C 2.5 2.0 3.3 Timer HOLD IDDHOLD(5) VDD1 Timer HOLD mode 1.8 to 5.5 22 95 mode FsX'tal=32.768 kHz crystal oscillation mode 1.8 to 3.6 7.5 35 Timer HOLD mode 5.0 22 60 FsX'tal=32.768kHz crystal oscillation mode 3.3 7.5 21 Ta=-10 to +50°C 7.5 7.5 7.5 7.5 7.5 7.5 7.5 Ta=-10 to +50°C 7.5 7.5 7.5 7.5 7.5 7.5 7.5 Ta=-10 to +50°C 7.5 7			-	LVD option selected					
*Ta=-10 to +50°C *LVD option selected *Ta=-10 to +50°C *LVD option selected *Timer HOLD mode *FsX'tal=32.768 kHz crystal oscillation mode *Timer HOLD mode *Timer HOLD mode *FsX'tal=32.768 kHz crystal oscillation mode *FsX'tal=32.768 kHz crystal oscillation mode *Timer HOLD mode *FsX'tal=32.768 kHz crystal oscillation mode *Ta=-10 to +50°C *Ta=-10 to +50°C		IDDHOLD(4)					3.0	5.7	μΑ
Timer HOLD IDDHOLD(5) VDD1 Timer HOLD mode 1.8 to 5.5 22 95 mode • FsX'tal=32.768 kHz crystal oscillation mode 1.8 to 3.6 7.5 35 consumption current (Note 9-1) IDDHOLD(6) Timer HOLD mode 5.0 22 60 • FsX'tal=32.768kHz crystal oscillation mode 3.3 7.5 21 • Ta=-10 to +50°C - Ta=-10 to +50°C - Ta=-10 to +50°C	Timer HOLD I			• Ta=-10 to +50°C					
mode • FsX'tal=32.768 kHz crystal oscillation mode 1.8 to 3.6 7.5 35 consumption current (Note 9-1) IDDHOLD(6) Timer HOLD mode 5.0 22 60 • FsX'tal=32.768kHz crystal oscillation mode 3.3 7.5 21 • Ta=-10 to +50°C		IDDHOLD(5)	V _{DD} 1	,					
consumption current (Note 9-1) IDDHOLD(6) Timer HOLD mode (FsX'tal=32.768kHz crystal oscillation mode (Note 9-1) 5.0 22 60 • FsX'tal=32.768kHz crystal oscillation mode (Note 9-1) 3.3 7.5 21		=======================================	100.						
current • FsX'tal=32.768kHz crystal oscillation mode 3.3 7.5 21 • Ta=-10 to +50°C - Ta=-10 to +50°C		IDDHOLD(8)	1						
(Note 9-1) • Ta=-10 to +50°C	current	10011010(0)							
(Note 9-2) 2.5 2.9 10					2.5		7.5 2.9	10	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

UART (Full Duplex) Operating Conditions at $Ta = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS}1 = V_{SS}2 = 0\text{V}$

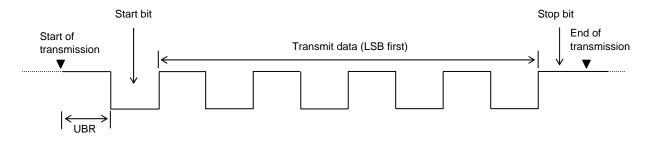
Deremeter	Cumbal Din/Damarka		Conditions		Specification			tion	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Transfer rate	UBR	UTX(P20) URX(P21)		1.8 to 5.5	16/3		8192/3	tCYC	

Data length: 7/8/9 bits (LSB first)

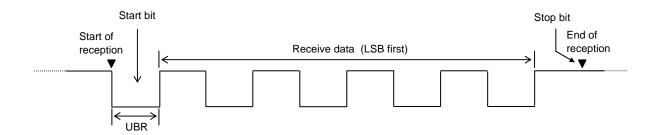
Stop bits: 1 bit (2-bit in continuous data transmission)

Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

• CF oscillation normal amplifier size selected (CFLAMP=0)

■MURATA

Nominal Frequency	Туре	Oscillator Name	Circuit Constant				Operating	Oscillation Stabilization Time		
			C1	C2	Rf	Rd	Voltage Range [V]	typ	max	Remarks
			[pF]	[pF]	[Ω]	[Ω]		[ms]	[ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	680	2.5 to 5.5	0.1	0.5	
					Open	1.0k	2.7 to 5.5	0.1	0.5	
	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	680	2.1 to 5.5	0.1	0.5	Internal C1,C2
10MHz					Open	1.0k	2.3 to 5.5	0.1	0.5	
	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	680	2.3 to 5.5	0.1	0.5	
					Open	1.0k	2.6 to 5.5	0.1	0.5	
	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	1.0k	2.0 to 5.5	0.1	0.5	
					Open	1.5k	2.1 to 5.5	0.1	0.5	
8MHz	LEAD	CSTLS8M00G53-B0	(15)	(15)	Open	1.0k	2.1 to 5.5	0.1	0.5	
					Open	1.5k	2.3 to 5.5	0.1	0.5	
6MHz	SMD	CSTCR6M00G53-R0	(15)	(15)	Open	1.5k	2.0 to 5.5	0.1	0.5	
					Open	2.2k	2.1 to 5.5	0.1	0.5	
	LEAD	CSTLS6M00G53-B0	(15)	(15)	Open	1.5k	2.0 to 5.5	0.1	0.5	
					Open	2.2k	2.2 to 5.5	0.1	0.5	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	1.8 to 5.5	0.2	0.6	
					Open	3.3k	1.9 to 5.5	0.2	0.6	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	1.8 to 5.5	0.2	0.6	
					Open	3.3k	1.9 to 5.5	0.2 0.6		

• CF oscillation low amplifier size selected (CFLAMP=1)

■MURATA

Nominal Frequency	Туре	Oscillator Name	Circuit Constant				Operating	Oscillation Stabilization Time		
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	Voltage Range [V]	typ [ms]	max [ms]	Remarks
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.0k	2.0 to 5.5	0.2	0.6	Internal C1,C2
					Open	2.2k	2.2 to 5.5	0.2	0.6	
		CSTCR4M00G53095-R0	(45)	5) (15)	Open	1.0k	1.9 to 5.5	0.2	0.6	
			(15)		Open	2.2k	2.0 to 5.5	0.2	0.6	
	LEAD	CSTLS4M00G53-B0	(15) (15)	(15)	Open	1.0k	2.3 to 5.5	0.2	0.6	
				(13)	Open	2.2k	2.3 to 5.5	0.2	0.6	
		CSTLS4M00G53095-B0	(1E)	(1E)	Open	1.0k	1.9 to 5.5	0.2	0.6	
		CG1EG4W00G55095-B0	(15)	(15)	Open	2.2k	2.0 to 5.5	0.2	0.6	

The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (See Fig. 3)

- Time till the oscillation gets stabilized after the CPU reset state is released
- Till the oscillation gets stabilized after the instruction for starting the main clock oscillation circuit is executed
- Till the oscillation gets stabilized after the HOLD mode is reset.
- Till the oscillation gets stabilized after the X'tal HOLD mode is reset with CFSTOP (OCR register, bit 0) set to 0

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

■EPSON TOYOCOM

Nominal Frequency	Туре	Oscillator Name	Circuit Constant				Operating	Oscillation Stabilization Time		D
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	Voltage Range [V]	typ [s]	max [s]	Remarks
32.768kHz	SMD	MC-306	9	9	Open	330k	1.8 to 5.5	1.4	4.0	Applicable CL value= 7.0pF

The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (See Fig. 3)

- Till the oscillation gets stabilized after the instruction for starting the subclock oscillation circuit is executed
- Till the oscillation starts and gets stabilized after the HOLD mode is reset when EXTOSC (OCR register, bit 6) is set to 1 and CFSTOP (OCR register, bit 0) is set to 1

(Notes on the implementation of the oscillator circuit)

- Oscillation is influenced by the circuit pattern layout of printed circuit board. Place the oscillation-related components as close to the CPU chip and to each other as possible with the shortest possible pattern length.
- Keep the signal lines whose state changes suddenly or in which large current flows as far away from the oscillator circuit as possible and make sure that they do not cross one another.
- Be sure to insert a current limiting resistor (Rd) so that the oscillation amplitude never exceeds the input voltage level that is specified as the absolute maximum rating.
- The oscillator circuit constants shown above are sample characteristic values that are measured using the SANYO-designated oscillation evaluation board. Since the accuracy of the oscillation frequency and other characteristics vary according to the board on which the IC is installed, it is recommended that the user consult the resonator vendor for oscillation evaluation of the IC on a user's production board when using the IC for applications that require high oscillation accuracy. For further information, contact your resonator vendor or SANYO Semiconductor sales representative serving your locality.
- It must be noted, when replacing the flash ROM version of a microcontroller with a mask ROM version, that their operating voltage ranges may differ even when the oscillation constant of the external oscillator is the same.

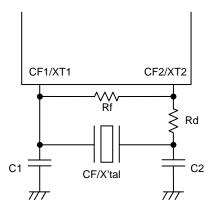


Figure 1 CF and XT Oscillator Circuit

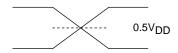
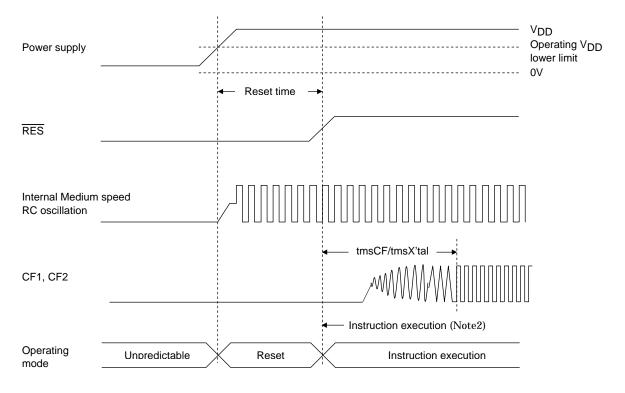
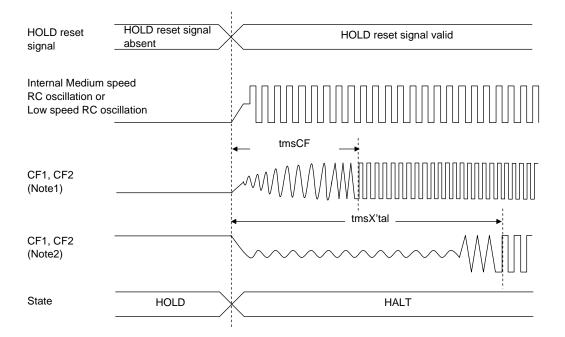


Figure 2 AC Timing Measurement Point



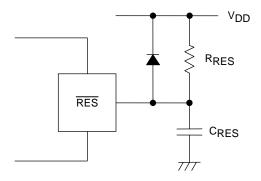
Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Note1: Mainclock oscillation circuit is selected. Note2: Subclock oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times



Note:

External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 4 Reset Circuit

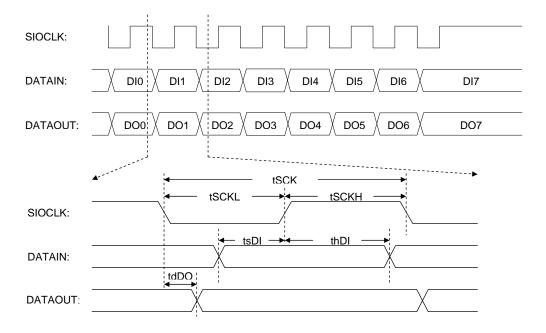


Figure 5 Serial I/O Output Waveforms

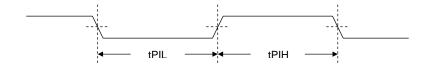


Figure 6 Pulse Input Timing Signal Waveform

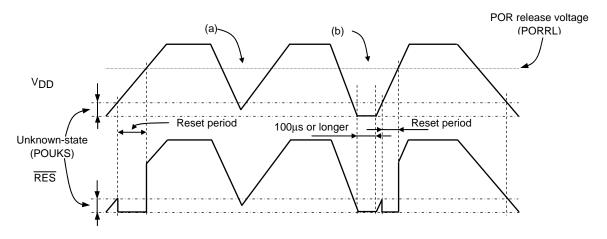


Figure 7 Waveform observed when only POR is used (LVD not used) (RESET pin: Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

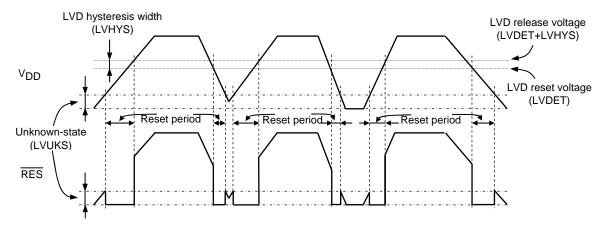


Figure 8 Waveform observed when both POR and LVD functions are used (RESET pin: Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

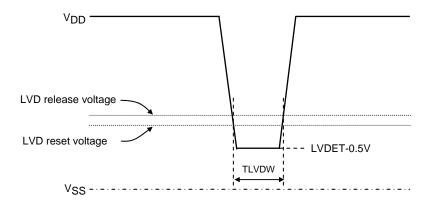


Figure 9 Low voltage detection minimum width (Example of momentary power loss/Voltage variation waveform)

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